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LOW GATE COUNT 3GPP CHANNELIZATION CODE GENERATOR

Field of the Invention

The present invention relates to generation of a 3GPP channelization code, and in particular, to a 3GPP channelization code generator with a low silicon area and low power consumption.

Background of the Invention

Code division multiple access (CDMA) is a technique that allows a communications system to accommodate a large number of system users. CDMA uses a spread spectrum modulation technique, where the signal energy of each channel is spread over a wide frequency band. Multiple channels each correspond to a different system user occupying the same frequency band.

Wideband code-division multiple access (WCDMA) is based on an ITU standard derived from code-division multiple access (CDMA). WCDMA is a third-generation mobile wireless technology. WCDMA can support mobile/portable voice, images, data, and video communications at up to 2 Mbps (local area access) or 384 Kbps (wide area access). Each analog input signal is converted into a digital signal that is spread spectrum coded for transmission over a broad range of frequencies.

User devices negotiate with a base station for a particular bandwidth when the user device is ready to transmit data. The user will be assigned a spreading factor and a code number to differentiate from other users. The spreading factor is associated with allocated bandwidth, and it typically a number that is an integral power of two from 1 to 256. The bandwidth is inversely proportional to the spreading factor. The code number is a number that is less than the spreading factor.

A channelization code is generated in response to the code number and the spreading factor. The data is multiplied by the channelization code after the channelization code is generated. The data is then scrambled. The data is broadcast after the data is scrambled.

Brief Description of the Drawings

Non-limiting and non-exhaustive embodiments of the present invention are described with reference to the following drawings.

FIG. 1 illustrates a circuit for uplink modulation that is arranged in accordance with aspects of the present invention.

FIG. 2 illustrates the 3GPP definition of a channelization code in the form of a matrix.

FIG. 3 illustrates the 3GPP definition of a channelization code in the form of a code tree.

FIG. 4 illustrates a channelization code generator circuit that is arranged in accordance with aspects of the present invention.

Detailed Description of the Preferred Embodiment

Throughout the specification and claims, the following terms take the meanings explicitly associated herein, unless the context clearly dictates otherwise. The meanings identified below are not intended to limit the terms, but merely provide illustrative examples for the terms. The meaning of "a," "an," and "the" includes plural reference, the meaning of "in" includes "in" and "on." The term "connected" means a direct electrical connection between the items connected, without any intermediate devices. The term "coupled" means either a direct electrical connection between the items connected, or an indirect connection through one or more passive or active intermediary devices. The term "circuit" means either a single component or a multiplicity of components, either active and/or passive, that are coupled together to provide a desired function. The term "signal" means at least one current, voltage, charge, temperature, data, or other signal. Referring to the drawings, like numbers indicate like parts throughout the views.

Briefly stated, the invention is related to generating a channelization code in response to a spreading factor and a code number. The code number is right justified to provide a right-justified code number. The right-justified code number is stored in an eight-bit register. An eight-bit binary counter is arranged to provide a binary count. The binary counter is reset when the binary count reaches a value equal

to the spreading factor minus one. A channelization logic circuit is configured to convert the binary count and the stored right-justified code number into the channelization code. According to one example, the channelization logic circuit comprises eight AND gates and eight XOR gates. A channelization code generator circuit may be integrated into an integrated chip that has a small silicon area and low power consumption.

FIG. 1 illustrates a circuit (100) for uplink modulation. Each of a plurality of data channels ($DPDCH_1$-$DPDCCH_6$) is multiplied by a channelization code ($C_{d,1}$ through $C_{d,6}$ respectively), and a gain (β_d) is applied to each of the channels. Each of the channelization codes ($C_{d,1}$ through $C_{d,6}$) is generated by a separate channelization code generator circuit (400). A control channel (DPCCH) is multiplied by a channelization code (Cc) and a gain (βc) is applied to the control channel. Channels $DPDCH_1$, $DPDCH_3$ and $DPDCH_5$ are summed to provide signal I, and channels $DPDCH_2$, $DPDCH_4$, $DPDCH_6$ and DPCCH are summed to provide signal Q. Signal Q is rotated by 90 degrees and summed with signal I to provide a combined signal. The combined signal is scrambled to provide a scrambled signal (S) by multiplying the combined signal by a scrambling code ($S_{dpch,n}$). The data is broadcast after the combined data from the data channels are scrambled.

Data that is broadcast via circuit 100 may be received by a mobile device via a circuit for downlink modulation (e.g. a rake receiver) (not shown). At least two channelization code generator circuits are required in the circuit for downlink modulation. One channelization code generator circuit is required for the data channel and one channelization code generator circuit is required for the control channel for a rake receiver with a single finger. Each additional data channel requires one additional channelization code generator circuit. To support 384Kbps, there are 3 data channels and one control channel for each finger. For optimal performance, the rake receiver has 6-8 fingers.

FIG. 2 illustrates the 3GPP definition of a channelization code in the form of a matrix. FIG. 3 illustrates the 3GPP definition of a channelization code in the form of a code tree.

A channelization code may be expressed as $C_{ch,SF,k}$, where SF is the spreading factor and k is the code number. The channelization code contains a set of elements, where the number of elements in the set is equal to the spreading factor. Each element of the channelization code consists of either 1 or -1. By definition, $C_{ch,1,0}$ has a single element, 1. $C_{ch,2,0}$ has two elements (1,1), and $C_{ch,4,2}$ has four elements (1, -1, 1, -1). The elements of a channelization code can be determined using the definition in FIG. 2, or using the code tree in FIG. 3.

The code tree illustrated in FIG. 3 may be used as follows. Progression from left to right leads to the next SF, where the SFs progress as integral powers of two (1, 2, 4, ... , 128, 256). Progression from top to bottom leads to the next code number (from 0 to SF-1). Progressing from left to right, each branch (the parent branch) branches into two separate branches (the descendant braches). The elements that comprises the first half of the elements of each branch are identical to the elements of the parent branch. For example, the parent branch for $C_{ch,2,0}$ = (1,1) divides into descendant branches $C_{ch,4,0}$ = (1,1,1,1) and $C_{ch,4,1}$=(1,1,-1-1). The first two elements of $C_{ch,4,0}$ and $C_{ch,4,1}$ are identical to the elements of $C_{ch,2,0}$. The elements that comprise the second half of the top descendent branch are also identical to the elements of the parent branch. For example, $C_{ch,2,0}$ = (1,1) and $C_{ch,4,0}$ = (1,1,1,1). The last two elements of $C_{ch,4,0}$ are identical to the elements of $C_{ch,2,0}$. Each of the elements that comprise the second half of the bottom descendent branch is the inverse of the corresponding element in the parent branch. For example, $C_{ch,2,0}$ = (1,1) and $C_{ch,4,1}$ = (1,1,-1,-1). The third element of $C_{ch,4,1}$ is the inverse of the first element in $C_{ch,2,0}$, and the last element of $C_{ch,4,1}$ is the inverse of the last element in $C_{ch,2,0}$.

FIG. 4 illustrates a channelization code generator circuit (400) that is arranged in accordance with aspects of the present invention. Circuit 400 comprises a binary counter circuit (402), a code logic circuit (404), a register circuit (406), and a channelization logic circuit (408). According to one example, channelization logic circuit 408 includes a plurality of AND gates (A0-A7) and a plurality of XOR gates (X0-X7).

Binary counter circuit 402 has a first input that is coupled to node N1, a second input that is coupled to node N37, and an eight-bit output. Each bit of the output (b0-b7) of binary counter circuit 402 is coupled to a respective one of nodes N19, N17, N15, N13, N11, N9, N7, and N5. Code logic circuit 404 has a first input that is coupled to node N1, a second input that is coupled to node N2, and an eight-bit output that is coupled to node N4. Register circuit 406 has an input that is coupled to node N4, and an eight-bit output. Each bit of the eight-bit output (b0-b7) of register circuit 406 is coupled to a respective one of nodes N6, N8, N10, N12, N14, N16, N18, and N20.

AND gate A0 has a first input that is coupled to node N5, a second input that is coupled to node N6, and an output that is coupled to node N21. AND gate A1 has a first input that is coupled to node N7, a second input that is coupled to node N8, and an output that is coupled to node N22. AND gate A2 has a first input that is coupled to node N9, a second input that is coupled to node N10, and an output that is coupled to node N23. AND gate A3 has a first input that is coupled to node N11, a second input that is coupled to node N12, and an output that is coupled to node N24. AND gate A4 has a first input that is coupled to node N13, a second input that is coupled to node N14, and an output that is coupled to node N25. AND gate A5 has a first input that is coupled to node N15, a second input that is coupled to node N16, and an output that is coupled to node N26. AND gate A6 has a first input that is coupled to node N17, a second input that is coupled to node N18, and an output that is coupled to node N27. AND gate A7 has a first input that is coupled to node N19, a second input that is coupled to node N20, and an output that is coupled to node N28.

XOR gate X0 has a first input that is coupled to node N21, a second input that is coupled to node N29, and an output that is coupled to node N30. XOR gate X1 has a first input that is coupled to node N22, a second input that is coupled to node N30, and an output that is coupled to node N31. XOR gate X2 has a first input that is coupled to node N23, a second input that is coupled to node N31, and an output that is coupled to node N32. XOR gate X3 has a first input that is coupled to node N24, a second input that is coupled to node N32, and an output that is coupled to node N33. XOR gate X4 has a first input that is coupled to node N25, a second input that is

coupled to node N33, and an output that is coupled to node N34. XOR gate X5 has a first input that is coupled to node N26, a second input that is coupled to node N34, and an output that is coupled to node N35. XOR gate X6 has a first input that is coupled to node N27, a second input that is coupled to node N35, and an output that is coupled to node N36. XOR gate X7 has a first input that is coupled to node N28, a second input that is coupled to node N36, and an output that is coupled to node N3.

Binary counter circuit 402 and code logic circuit 404 are each configured to receive a spreading factor signal at node N1. According to one example, the spreading factor signal is an eight-bit binary signal that corresponds to SF. Binary counter circuit 402 is further configured to receive a clock signal at node N37. Code logic circuit 404 is further configured to receive a code number signal (code) at node N2. XOR gate X0 is configured to receive a signal that corresponds to a logical level of zero at node N29.

Binary counter circuit 402 is illustrated as an eight-bit binary counter. The binary counter circuit (402) is arranged as a modulo SF binary counter. The binary counter circuit (402) counts from 0 to SF-1 in response to the clock signal. The binary counter circuit (402) rolls back to 0 the next clock after the count reaches SF-1. Binary counter circuit 402 is configured to provide the binary count as a binary count signal at the output of binary counter circuit 402.

Code logic circuit 404 is arranged to provide a right justified code number signal (rjcode) in response to the SF signal and the code number signal (code). Code logic circuit 404 is arranged to evaluate the number of valid bits in the code number according to the SF. The number of valid bits (N) is equal to $\log_2$ (SF). For example, an SF of 2 corresponds to one valid bit, an SF of 4 corresponds to two valid bits, and an SF of 8 corresponds to three valid bits. The most significant valid bit from the code number signal (code) is moved to the bit 7 position of the right justified code number signal (rjcode). All bits other than the N most significant bits are adjusted to zero.

For example, rjcode corresponds to 01100000 when the channelization code corresponds to $C_{ch,8,3}$. In this example, three bits are used since the SF is 8, the

code number corresponds to 011, and the most significant bit is adjusted to bit 7, so that bits 7, 6, and 5 corresponds to 0, 1, and 1 respectively. All bits other than the three most significant bits are adjusted to zero.

Register circuit 406 is arranged to store the right-justified code number. Register circuit 406 is configured to provide the stored right-justified code number as a stored code number signal at the output of register circuit 406.

Channelization logic circuit 408 is configured to provide the channelization code signal in response to the stored code number signal and the binary count signal. Channelization logic circuit 408 is configured to provide the channelization code signal in a serial manner. The first element of the channelization code is generated at a first clock pulse (i.e. when the binary count corresponds to zero). Each subsequent element of the channelization code is generated at each subsequent clock pulse (i.e. when the binary count increments). Channelization logic circuit 408 provides the first element of the channelization code again after all of the elements of the channelization code have been generated (i.e. when the binary count has reset to zero after reaching SF-1). A digital value of 0 corresponds to a channelization code element of "-1", while a digital value of 1 corresponds to a channelization code element of "1".

According to a further example, binary counter circuit 402 includes a digital comparator that is configured to compare the binary count to SF-1. According to this example, an output of the digital comparator is coupled to a reset input of the binary counter such that the binary counter is reset to 0 when the binary count corresponds to SF-1.

According to one example, binary counter circuit 402 is configured to receive a frame reset signal. The binary counter is reset to 0 when either the frame reset signal corresponds to an active level or the signal provided by the digital comparator output corresponds to an active level. For example, binary counter circuit 402 may further include an OR gate having a first input, a second input, and an output. The first input is configured to receive the frame reset signal, the second input is coupled to the

output of the digital comparator, and the output of the OR gate is coupled to the reset input.

According to an alternative example, binary counter circuit 402 does not receive a frame reset signal. Circuit 400 is configured to receive signals code, clock, and SF such that the binary count always corresponds to zero after the next clock when the code number or the SF changes.

An example of generation of the channelization code for $C_{ch,2,1}$ proceeds as follows. Code logic circuit 404 provides signal rjcode as 10000000 in response to the SF signal (which corresponds to 2) and the code number signal (which corresponds to 1). Register circuit 406 stores 10000000 as the stored code number in response to the next clock. Initially, the binary count corresponds to 00000000. The voltages at nodes N21-N27 each correspond to a logical level of zero, because bits 1-7 of the binary count signal each correspond to 0 and bits 0-6 of the stored code number signal each correspond to zero. AND gate A7 provides a voltage that corresponds to a logical level of zero at node N28, since bit 0 of the binary count signal corresponds to 0. The voltage at node N3 corresponds to a logical level of zero since both inputs of each of the XOR gates X0-X7 correspond to zero. The first element of the channelization code is generated as "1" since the logical level associated with the voltage at node N3 corresponds to zero.

The binary count increments from 00000000 to 00000001 in response to the clock signal. The voltage at nodes N21-N27 and N36 each correspond to a logical level of zero since bits 1-7 of the binary count signal and bits 0-6 of the stored code number signal are unchanged since the previous clock. AND gate A7 provides a voltage that corresponds to a logical level of one at node N28, since bit 0 of the binary count signal corresponds to 1 and bit 7 of the stored code number corresponds to 1. XOR gate X7 provides a voltage that corresponds to a logical level of 1 at node N3, since the voltage at node N28 corresponds to a logical level of 1 and the voltage at node N37 corresponds to a logical level of 0. The second element of the channelization code is generated as "-1" since the logical level of the voltage at node N3 corresponds to 1.

The binary count returns to 00000000 after the next clock, and the process repeats until a new code number is received.

The above specification, examples and data provide a complete description of the manufacture and use of the composition of the invention. Since many embodiments of the invention can be made without departing from the spirit and scope of the invention, the invention resides in the claims hereinafter appended.